MAC CONTROLLED SLEEP MODE/WAKE-UP MODE WITH STAGED WAKE-UP FOR POWER MANAGEMENT

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ABSTRACT OF THE DISCLOSURE

[043]   A power management scheme for a wireless communications device processor substantially implemented on a single CMOS integrated circuit is described. By incorporating controls for sleep and wake-up mode transitions in the processor's control logic, improved power savings with reduced latency is provided, obviating the need for hardware-focused solutions with elaborate signaling mechanisms. A fully integrated power management with staged wake-up operations controlled by the MAC solution consumes less power than the conventional wireless LAN solutions in standby mode.